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Enhanced Wafer Overlay Residuals Control; Deep Sub-Nanometer at Sub-Millimeter Lateral Resolution

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ABSTRACT

The introduction of advanced technology nodes in deep UV (DUV) lithography (litho), involving multiple litho steps, has tightened the wafer on-product overlay specifications [1]. The industry trend already pushes the overlay requirements to the sub-nanometer regime (and so the mask registration requirements tightens as well). In the most general view, wafer on-product overlay errors are a combination of intra-field (within field) and inter-field (field-to-field) errors. A given litho layer intra-field overlay error includes several systematic sources, such as scanner lens-to-lens residuals and mask writer residuals. Parallel to the nodes and litho techniques advancing, the ability to accurately measure overlay at high lateral resolution have being successfully introduced, both at wafer and mask side.

The recent developments in scanner technology improved the ability to control intra-field overlay at high-order across the exposure field. However, this is still in several millimeter lateral resolution control ability at its best, leaving residual errors in the sub-millimeter to few millimeter regime without the ability to further suppress them to the target specification, nevertheless, not to the sub-nanometer magnitude.

In this work, we have empirically evaluated the ZEISS state-of-the-art mask tuning solution named ForTune ERC (Enhanced Registration Control). This solution is based on laser processing of the mask bulk by the ZEISS ForTune tool. It allows to suppress few nanometer overlay residuals (post the scanner best-can-do) down to deep sub-nanometer, all even at sub-millimeter sampling resolution (x1 wafer level) and low-to-high residuals modulating frequency.

For the sake of this study, we have used a dual-image mask to form one overlay signature at wafer side. Two wafers have been exposed prior to the laser-based tuning of the mask bulk; the wafers overlay error was measured and used as an initial overlay problem to begin with. A second exposure of two additional wafers was performed post the problem-solving by the ERC model and the consequent mask laser-based tuning. The pre/post wafers were then compared to examine the improvement in overlay at wafer side. CD uniformity (CDU) data has been collected as well, to confirm no degradation in CDU due to the ForTune ERC process.

The combination of this advanced method of intra-field control with high-order correction per exposure (CPE) by the scanner, provides an efficient co-optimized solution to tightly control the overlay of existing and future nodes at DUV litho.

Keywords: ERC, ForTune, Overlay, Registration, DUV, Mask, Laser, Lithography, Metal, Super Nova

1. INTRODUCTION

DUV litho processes get more and more demanding as technology nodes shrinks and as the high-volume manufacturing (HVM) is ramping up with today's layers generation. Specifically, with regards to overlay performance, the fight for every sub-nanometer fragment out of the overall (litho) residuals gets more and more attention. This, along with the evolvement of on-product overlay sampling strategies and metrology techniques advancing, finally allows pushing the layer-to-layer overlay to the sub-nanometer regime. In the most general way, at the moment that the intra field overlay

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problem has been sampled and well identified, the first level approach for suppression of residuals, depending on the problem magnitude and spatial frequency nature, may be:

1. Feed-backwards to the scanner and compensate using its different knobs

2. Manufacture new mask which counter compensate this problem

Those two are both valid and commonly used by integrated circuits (IC) manufacturers. However, in addition to the associated logistics, cost and long cycle time, along with other drawbacks in the HVM flow, they are both limited in spatial resolution and yield a limited residuals suppression rate, still leaving up to few nanometers overlay residuals. In this work we evaluated an alternative method; mask level tuning with laser acting on the mask bulk (glass) volume to control and suppress the overlay residuals down to sub-nanometer level at high (sub-millimeter) sampling resolution/spatial frequency as input. This method may act in a co-optimized approach with either #1 or #2 above (or both combined) to even further optimize workflow towards best productivity and device performance.

1.1 Mask tuning; ForTune concept explanation

The concept of mask (bulk) tuning by laser treatment has been discussed in detail in previous works [2, 3]. This technology, aka as RegC®, is a well-established HVM solution which is being used by advanced (IC) manufacturers for many years already. The ForTune system uses a pulsed laser to generate micrometer-sized deformation elements (aka pixels) inside the mask fused silica bulk. Those elements lead to a well-controlled and accurately predicted deformation of the bulk in a predefined direction and magnitude (forming "working mode"). The ForTune tool, being a state-of-the-art system, is pre-calibrated to hold 4 fundamental working modes which allows 4 different fundamental deformation of the mask bulk and hence 4 different direction to displace the (attached-to-bulk) patterned absorber. Figure 1a illustrates how the laser beam is directed via the mask backside (absorber down) to be finally focused inside the mask bulk. Figure 1b shows top view image of deformation elements formed by this laser beam (2 examples). Figure 2 illustrates the 4 fundamental mask pattern/wafer overlay control directions.

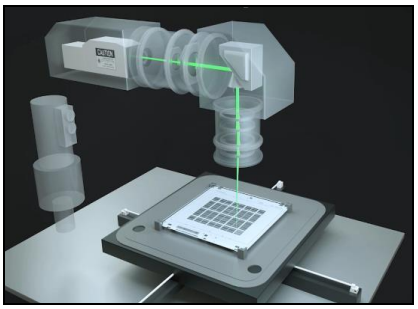

Figure 1a. ForTune laser beam focused inside the mask quartz bulk

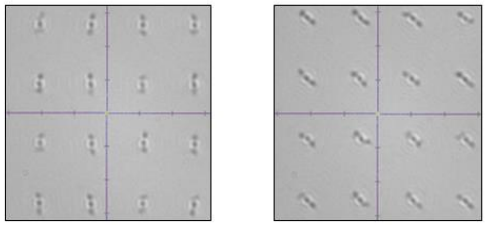

Figure 1b.Top view of laser-formed micrometer sized deformation element inside the mask bulk (2examples)

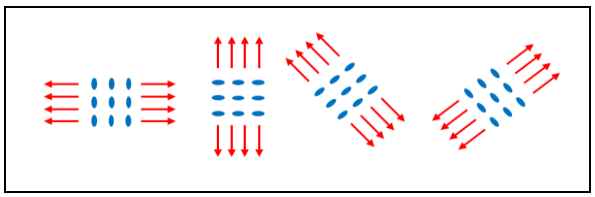

Figure 2. Illustration of the deformation elements (blue ellipse) and the associated direction of displacement in the mask absorber level (red arrows), forming 4 fundamental working modes

1.2 Enhancement to sub-nanometer residuals

The image displacement properties of the four ForTune working modes are being considered by the ERC model when solving overlay problem residuals by physical model. The recently developed "Enhanced Registration Correction" model (ERC model) considers several aspects associated with both the laser process parameters and mask bulk parameters, which so far were neglected or only approximated. This enhancement, along with the utilization of much higher computational power over advanced computational engine (ZEISS FAVOR), allows controlling the problem residuals at sub-millimeter spatial resolution and with significantly improved accuracy. Consequently, the ForTune ERC process offers advanced laser beam control, accompanied by an enhanced problem-solving model, resulting in sub-nanometer overlay residuals at wafer level.

This solution works in co-optimization with the available scanners knobs to address overlay errors as been studied in previous work [4]. Its key target is to transform overlay non-correctable error (residuals) into a scanner-correctable error, leaving a suppressed overlay problem after the scanner compensation; Figure 3 illustrates this transformation flow. The ERC model is flexible with definition of the scanner compensation type, which needs to be considered per litho case (linear or higher-order polynomial compensation).

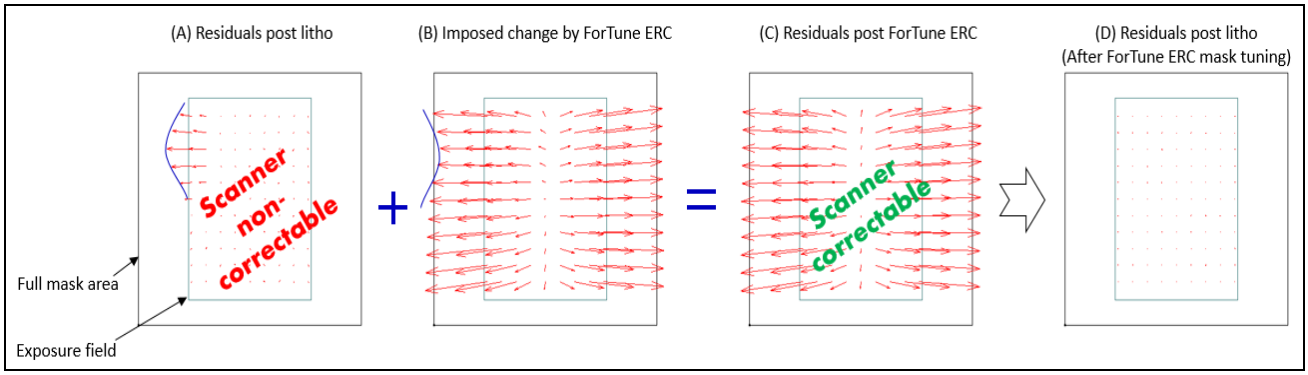

Figure 3. Wafer overlay residuals synthetic example, represented in mask level (A), Imposed image placement change to the mask as computed by ERC model and applied by ForTune process (B), Resulted scanner-correctable (overlay) error (C), Overlay residuals after mask tuning and litho steps (D).

2. EXPERIMENTAL DETAILS

2.1 Goals

This study focused on two key goals:

Goal 1: Demonstrate the ForTune ERC ability to reduce wafer overlay problem down to sub-nanometer residuals.

Goal 2: Confirm that there is no negative impact on the critical dimension uniformity (CDU)

As for goal 2, the concern relates to the properties of the deformation elements which slightly back-scatter light outside of the scanner pupil. This leads to minor dose reduction in relative to the dose level prior to the ForTune process. During standard preparation for exposure step, the scanner optimal dose is been adjusted to compensate for this effect. However, potential local variations in the back scattering of the pixels might cause local dose changes at wafer which in the end might negatively impact the CD uniformity (CDU), hence the ERC process is designed and controlled to have no impact on CDU ("CDU neutral"). For examination of this, CDU has been measured before and after the ForTune ERC process although the (overlay) solution is considering neutral effect on CDU in advance.

2.2 Workflow

For the sake of this study, we have used a dual-image (bottom, top) mask (see Fig. 5) to form one overlay signature at wafer side. The demonstration in this study consists of the following steps:

a. Expose bottom image over 4 wafers; A, B, C and D

b. Expose top image over 2 wafers; A and B

c. Measure pre-overlay (top-to-bottom image) over wafers A and B and pre-CDU (top image)

d. Compute ERC solution for the pre-overlay residuals (c)

e. Run ForTune ERC process to apply the solution (d) over the mask

f. Expose top image over 2 wafers; C and D

g. Measure post overlay (top-to-bottom image) over wafers C and D and post CDU (top image)

h. Analyze overlay pre (c) versus overlay post (g) to examine goal 1

i. Analyze CDU pre (c) versus CDU post (g) to examine goal 2

As for overlay measurements, 22 exposure fields were measured in each step (pre (c) and post (g)) consisting of 11 scan up direction and 11 scan down direction fields (representing a sub set out of standard HVM wafer exposure case). Overlay residual signature for the ERC solution (d) has been generated out of the average of the 22 exposure fields, same practice has been repeated for post overlay residual signature generation (g). As for CDU error, 10 fields have been averaged for pre (c) and 10 for post (g) process analysis. Figure 4 illustrates these experimental steps (a-i) in a block diagram.

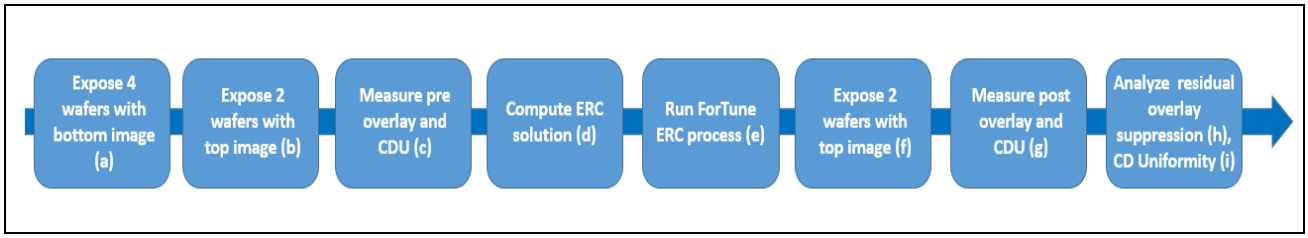

Figure 4. Overview of this study workflow

2.3 Test mask and wafer metrology

The mask used in this study is a standard 6" quartz 6% attenuated phase shift mask (without pellicle) containing two images that are used in DUV (193nm) immersion lithography. Each image size is 104mm x 64mm, the image centers are located at ±34mm on Y-axis with respect to center of the mask plate. The bottom image, Metal 1A, is used to pattern the first layer and top image, Metal1B, is used to pattern the second layer for a Litho-Etch-Litho-Etch (LELE) process forming pattern of 48 nm pitch targeted to be 24 nm CD trenches. Figure 5 shows an overview of the dual image mask layout (Cr side up orientation). This mask is used in back end of line (BEOL) processes and contains a large number of metrology targets for CD and overlay measurements.

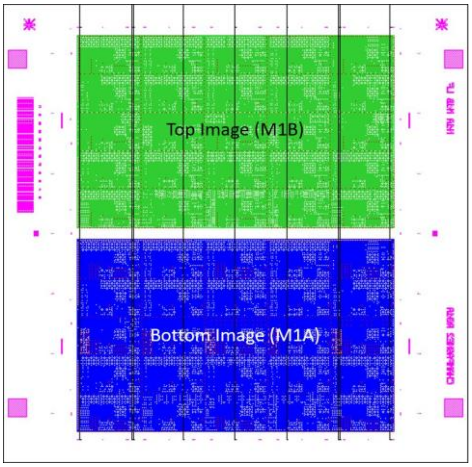

Figure 5. Overview of the dual image mask layout used in this study (Cr side up orientation)

Four 300 mm Si wafers were prepared for this study. IMEC SuperNova2 process stack which consists of seven different stack deposition for metal-1 (M1) patterning was used. Figure 6 shows the schematic representation of the stacks and process flow. The process contains two lithography steps. After the stack deposition, M1A image was exposed by using ASML 1970i TWINSCAN scanner. All the lithography steps were performed by using same chuck to avoid chuck to chuck variation. M1A image was etched into 20 nm hard mask oxide layer. The bottom grating for the overlay targets were defined to achieve a CD of 24 nm in this layer. The last step of the process is M1B image exposure where the top grating is patterned at 38 nm CD trench in the 85 nm resist. The bottom and top gratings were separated by 40 nm Spin-on-Glass (SoG) and 100 nm Spin-on-Carbon (SoC) layers.

Figure 6. Schematic representation of the lithography process flow.

The overlay measurements were performed on ASML Yieldstar-250D, a diffraction-based overlay (DBO) metrology tool. An interlaced design of µDBO overlay targets in the size of 16µm x 16µm were chosen to perform overlay measurements. Figure 7 shows an image of such overlay target design. The target contains horizontal and vertical gratings with a pitch of 600 nm.

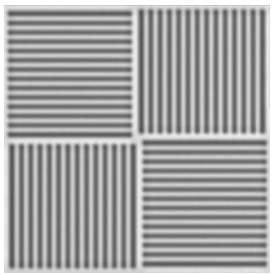

Figure 7. Image of the interlaced µDBO overlay target.

A high density of sampling scheme has been defined for measurements to monitor along the slit overlay variations. 70 overlay targets were distributed through slit direction in 4 slits structure, forming 280 intra-field measurement points with 0.37 mm step in X and 3.18-mm step in Y (x1), measured over 22 fields. The fields were selected considering scan up (11) and scan down (11) directions during the exposure. Figure 8 shows wafer spread map and intra-field sampling scheme for the overlay measurements.

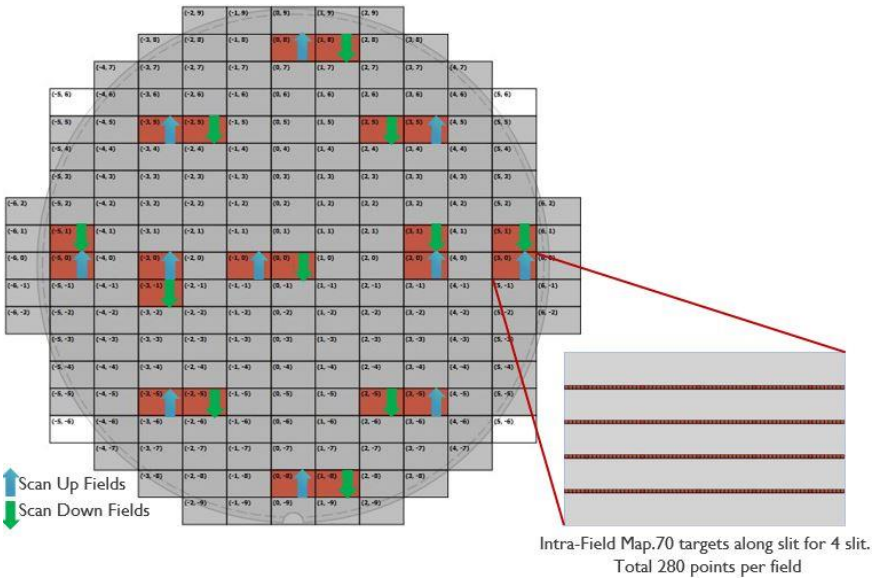

Figure 8. Wafer-spread sampling scheme (22 fields) used for overlay measurements, 280 (4x70) points per field.

CD measurements have been done on an anchor feature, which consists of lines and spaces. The pitch of the lines is 96 nm and width is 24 nm. The anchor feature is located 50 µm away from the µDBO overlay target. The CD measurements were performed on Hitachi CG6300 automated CD-SEM tool after M1B lithography to examine if there were any effects of the mask laser-based tuning on wafer CD. Same sampling scheme as overlay measurements were used except for the number of sampled fields which was reduced to 10 (5 scan-up, 5 scan-down) due to measurement time considerations.

3. RESULTS

3.1 Overlay residuals reduction (Goal 1 results)

Figure 9 shows the wafer overlay residuals (formed by top-to-bottom mask image) plots at mask level (x4) before and after the ForTune ERC process under scanner standard linear compensation. This demonstration showed further suppression of the overlay problem beyond the scanner best-can-do by ~ 50% down from > 1 nanometer to ~ 0.5 nanometer (x1) residuals in this studied case. Looking at the per-row direction of overlay error it seems that some

overshoot occurred in this demonstration (change in the error Y direction between before and after process). This is due to lack of process calibration step in this demonstration. Overcoming this kind of overshoot is possible by running one-time process calibration per HVM environment, leading finally to even better suppression of the overlay residuals.

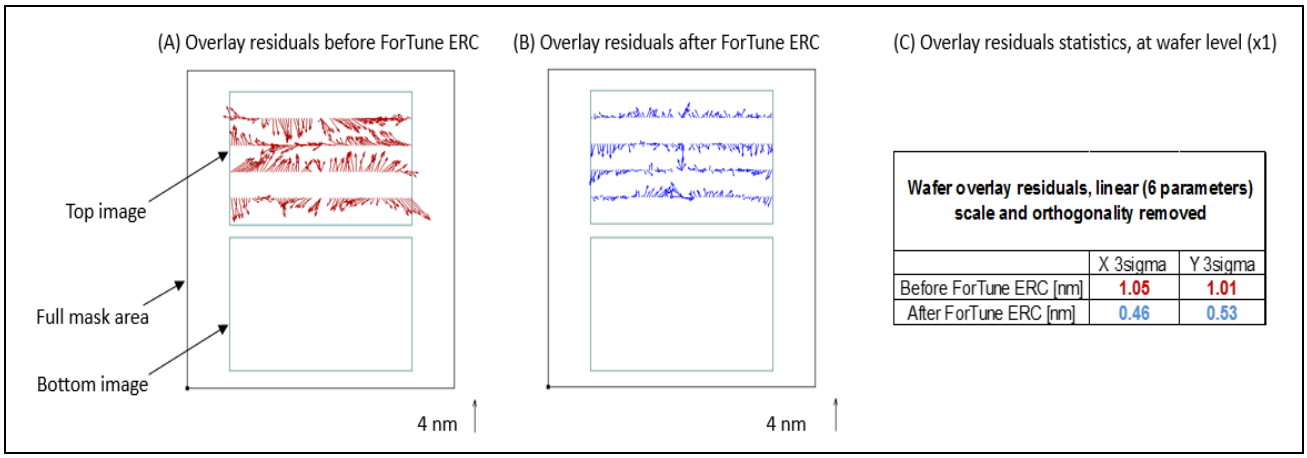

Figure 9. Overlay residuals before ForTune ERC (A), after ForTune ERC (B) and statistics (C)

Furthermore, despite the dense sampling (0.37 mm step in X at wafer level), it seems that this process has nicely controlled the overlay residuals even at locations with direction-contradicting error, exhibiting high spatial variance (frequency) of the problem to begin with. Figure 10 shows an example of several locations (selected out of figure 9 plots) with direction-contradicting error (before process) which have been suppressed and are now direction-similar as well.

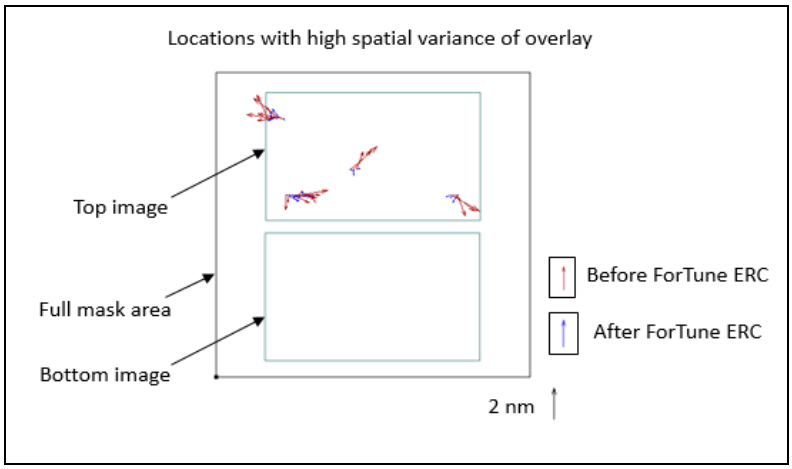

Figure 10. Overlay residuals before ForTune ERC with high spatial frequency (brown) and suppressed (magnitude and frequency) after ForTune ERC (blue)

3.2 Neutral effect on CDU error (Goal 2 results)

In order to examine if there are mask tuning process related effects on CDU error, the sampled 10 exposure fields were averaged to demonstrate preprocess CDU error on top layer (M1B) litho. The same practice has been repeated on M1B litho for the post mask process. The difference of post-to-pre CD in each location (280 intra field locations) was then plotted against the slit direction shown in mean-to-target representation (see Fig. 11). Obviously, this CD difference was

expected to be different from zero due to the litho and metrology inherent repeatability, hence, the examination of the CD difference was done under these repeatability boundaries. Each single location repeatability was defined as 3-sigma over 10 fields; A representative repeatability boundary has been computed as square root of the pre and post CD measurement average repeatability (over 280 locations). Figure 11 shows the CD difference along the slit direction examined under the repeatability boundaries. Overall, considering the repeatability boundaries there is no observable change in CDU residuals due to the mask tuning process.

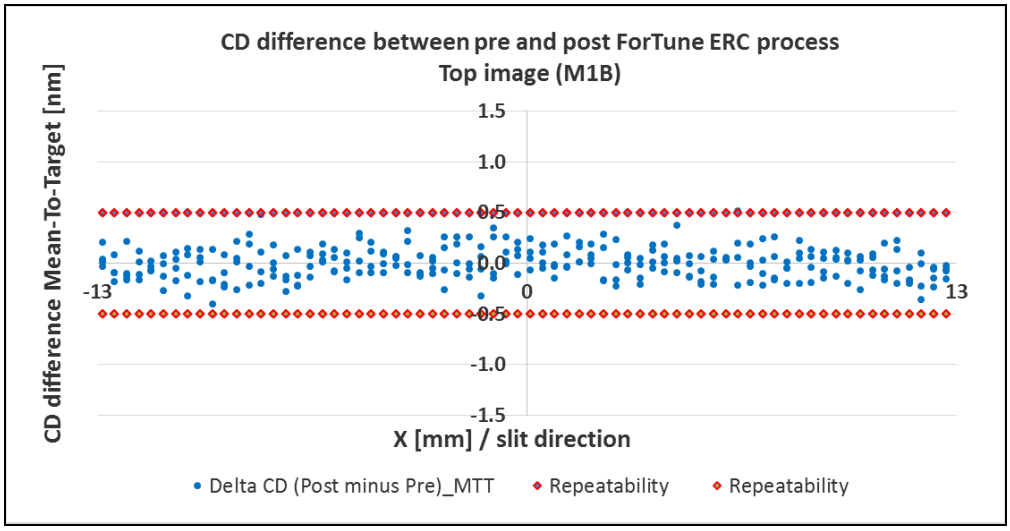

Figure 11. CD difference against litho and metrology repeatability

4. DISCUSSION

In this work, we have studied the new Enhanced Registration Correction Process (ERC) which allows further reduction of overlay residuals down to sub-nanometer regime by mask tuning. The discussed process acts complementary to the litho scanner knobs and offers performance beyond the scanner best-can-do. The enhancement in overlay suppression is achieved by adding one more process step to the standard litho steps at HVM; mask tuning by laser which is being fed backwards with the overlay residuals at wafer side. This essentially saves the need for mask re-manufacturing as well.

This extra step, which typically takes a few hours to run in an automated way from solution computation until mask return to HVM line, may suppress few nanometers overlay residuals down to sub-nanometer. All at wide low-to-high spatial frequency variance of the overlay error magnitude and direction and in dense sampling schemes as demonstrated in this work.

This mask tuning technology synergy with production lines and lack of side effects have been studied several times in the past by end users, prior to introduction in HVM several years ago [5]. In this work we have demonstrated neutral effect on CDU while applying this well controlled ForTune ERC process to the mask bulk. The combination of this advanced method of intra-field control with high-order correction per exposure (CPE) by the scanner, provides an efficient co-optimized solution to tightly control the overlay of existing and future nodes at DUV litho.

5. CONCLUSIONS

The recently released ForTune ERC process has been demonstrated to achieve sub-nanometer overlay residuals at wafer side, showing ~ 50% suppression of the residual error in this demonstration with no observable impact on CDU. This method offers enhanced overlay residuals suppression beyond the scanner best-can-do or other alternative approaches such as mask re-writing.

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